Amendments to the Claims:

Please cancel, without prejudice, non-elected claims 41-52 and 69-72 and add new dependent claims 73-84. This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

(Claims 1-24 have been cancelled.)

25.(Original) A method of simulating the operation of a circuit, comprising:

providing a simulation model of the circuit;

selecting a set of frequency points;

simulating the response of the circuit for a subset of the frequency points using the simulation model, said subset comprising a first group and a distinct second group, wherein each frequency point of said first group lies between a pair of frequency points in said second group of frequency points;

interpolating the response of the circuit for the first group of frequency points from the simulated values of the second group of frequency points;

comparing the simulated response with the interpolated response for the first group of frequency points, wherein if the difference between the simulated value and the interpolated value of a first point in the first group exceeds a bound, an additional frequency point is added to the second group, the additional point lying between the same pair of frequency points in said second group as the first point;

iteratively repeating the interpolating and comparing until the difference between the simulated value and the interpolated value of each point in the first group do not exceeds the bound; and

determining the response of the circuit for frequency points not in the subset from the interpolated response.

26.(Original) The method of claim 25, wherein said response is interpolated and simulated in the Y response parameter representation.

27.(Original) The method of claim 25, wherein the interpolating is a cubic spline interpolation.

28.(Original) The method of claim 25, wherein the circuit is a sub-circuit representation of a non-linear device.

29.(Original) The method of claim 28, wherein the non-linear device is a MOSFET.

30.(Original) The method of claim 29, wherein the set of frequency points includes frequencies greater than 10^9 hertz.

31.(Original) The method of claim 30, wherein the number of elements in the set of frequency points is larger than the number of elements in the subset of frequency points by more than a factor of ten.

(Claims 32-64 have been cancelled.)

65.(Original) A computer readable storage device embodying a program of instructions executable by a computer to perform a method of simulating the operation of a circuit, said method comprising:

providing a simulation model of the circuit;

selecting a set of frequency points;

simulating the response of the circuit for a subset of the frequency points using the simulation model, said subset comprising a first group and a distinct second group, wherein each frequency point of said first group lies between a pair of frequency points in said second group of frequency points;

interpolating the response of the circuit for the first group of frequency points from the simulated values of the second group of frequency points;

comparing the simulated response with the interpolated response for the first group of frequency points, wherein if the difference between the simulated value and the interpolated value of a first point in the first group exceeds a bound, an additional frequency point is added to the second group, the additional point lying between the same pair of frequency points in said second group as the first point;

iteratively repeating the interpolating and comparing until the difference between the simulated value and the interpolated value of each point in the first group do not exceeds the bound; and

determining the response of the circuit for frequency points not in the subset from the interpolated response.

66.(Original) The computer readable storage device of claim 65, wherein the circuit is a sub-circuit representation of a MOSFET.

67.(Original) A method for transmitting a program of instructions executable by a computer to perform a process of simulating the operation of a circuit, said method comprising:

transmitting to a user a program of instructions; and

enabling the user device to perform, by means of such program, the following process:

providing a simulation model of the circuit;

selecting a set of frequency points;

simulating the response of the circuit for a subset of the frequency points using the simulation model, said subset comprising a first group and a distinct second group, wherein each frequency point of said first group lies between a pair of frequency points in said second group of frequency points;

interpolating the response of the circuit for the first group of frequency points from the simulated values of the second group of frequency points;

comparing the simulated response with the interpolated response for the first group of frequency points, wherein if the difference between the simulated value and the interpolated value of a first point in the first group exceeds a bound, an additional frequency point is added to the second group, the additional point lying between the same pair of frequency points in said second group as the first point;

iteratively repeating the interpolating and comparing until the difference between the simulated value and the interpolated value of each point in the first group do not exceeds the bound; and

determining the response of the circuit for frequency points not in the subset from the interpolated response.

68.(Original) The method of claim 67, wherein the circuit is a sub-circuit representation of a MOSFET.

(Claims 69-72 have been cancelled.)

73.(New) The computer readable storage device of claim 65, wherein said response is interpolated and simulated in the Y response parameter representation.

74.(New) The computer readable storage device of claim 65, wherein the interpolating is a cubic spline interpolation.

75.(New) The computer readable storage device of claim 65, wherein the circuit is a sub-circuit representation of a non-linear device.

76.(New) The computer readable storage device of claim 65, wherein the non-linear device is a MOSFET.

77.(New) The computer readable storage device of claim 65, wherein the set of frequency points includes frequencies greater than 10^9 hertz.

78.(New) The computer readable storage device of claim 65, The method of claim 30, wherein the number of elements in the set of frequency points is larger than the number of elements in the subset of frequency points by more than a factor of ten.

79.(New) The method of claim 67, wherein said response is interpolated and simulated in the Y response parameter representation.

80.(New) The method of claim 67, wherein the interpolating is a cubic spline interpolation.

81.(New) The method of claim 67, wherein the circuit is a sub-circuit representation of a non-linear device.

82.(New) The method of claim 67, wherein the non-linear device is a MOSFET.

83.(New) The method of claim 67, wherein the set of frequency points includes frequencies greater than 10^9 hertz.

84.(New) The method of claim 67, wherein the number of elements in the set of frequency points is larger than the number of elements in the subset of frequency points by more than a factor of ten.